Advanced Information

SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

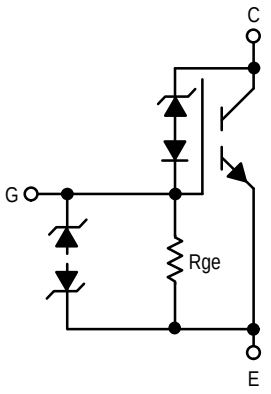
MGP20N40CL

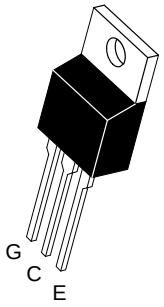
20 AMPERES
VOLTAGE CLAMPED
N–CHANNEL IGBT
$V_{ce(on)}$ = 1.8 VOLTS
400 VOLTS (CLAMPED)

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Drain Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability

TMOS®





CASE 221A–06, Style 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous @ T_C = 25°C	I_C	20	Adc
Reversed Collector Current – pulse width < 100 μs	I_{CR}	12	Apk
Total Power Dissipation @ T_C = 25°C (TO–220)	P_D	150	Watts
Electrostatic Voltage — Gate–Emitter	ESD	3.5	kV
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

UNCLAMPED INDUCTIVE SWITCHING CHARACTERISTICS

Single Pulse Collector–Emitter Avalanche Energy @ Starting T_J = 25°C @ Starting T_J = 150°C	E_{AS}	 550 150	mJ

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–to–Emitter Breakdown Voltage (I_{Clamp} = 10 mA, T_J = –40 to 150°C)	B_{VCES}	370	405	430	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 350 V, V_{GE} = 0 V, T_J = 150°C)	I_{CES}	—	—	500	μA
(V_{CE} = 15 V, V_{GE} = 0 V, T_J = 150°C)		—	—	100	
Resistance Gate–Emitter (T_J = –40 to 150°C)	R_{GE}	10k	16k	30k	Ω
Gate–Emitter Breakdown Voltage (I_G = 2 mA)	B_{VGES}	11	13	15	±V
Collector–Emitter Reverse Leakage (V_{CE} = –15 V, T_J = 150°C)	I_{CES}	—	—	50	mA
Collector–Emitter Reversed Breakdown Voltage (I_E = 75 mA)	B_{VCER}	26	40	120	V
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mA)	$V_{GE(th)}$	1.0	1.7	2.2	V
(V_{CE} = V_{GE}, I_C = 1 mA, T_J = 150°C)		0.75	—	1.8	
Collector–Emitter On–Voltage (V_{GE} = 5 V, I_C = 5 A)	$V_{CE(on)}$	—	1.1	1.4	V
(V_{GE} = 5 V, I_C = 10 A)		—	1.4	1.9	
(V_{GE} = 5 V, I_C = 10 Adc, T_J = 150°C)		—	1.4	1.8	
Forward Transconductance (V_{CE} > 5.0 V, I_C = 10 A)	g_{fs}	10	18	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	2800	—	pF
Output Capacitance	C_{oss}	—	200	—	
Transfer Capacitance	C_{rss}	—	25	—	
SWITCHING CHARACTERISTICS (1)					
Total Gate Charge	Q_g	—	45	80	nC
Gate–Emitter Charge	Q_{gs}	—	8.0	—	
Gate–Collector Charge	Q_{gd}	—	20	—	
Turn–Off Delay Time	$t_{d(off)}$	—	14	—	μs
Fall Time	t_f	—	4.0	—	
Turn–On Delay Time	$t_{d(on)}$	—	2.0	—	μs
Rise Time	t_r	—	6.0	—	

(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)

(V_{CC} = 280 V, I_C = 20 A, V_{GE} = 5 V)

(V_{CC} = 320 V, I_C = 20 A, L = 200 μH, R_G = 1 KΩ)

(V_{CC} = 14 V, I_C = 20 A, L = 200 μH, R_G = 1 KΩ)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

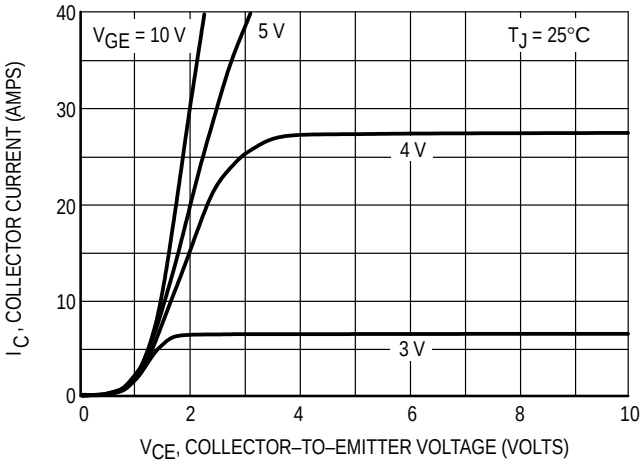


Figure 1. Output Characteristics, T_J = 25°C

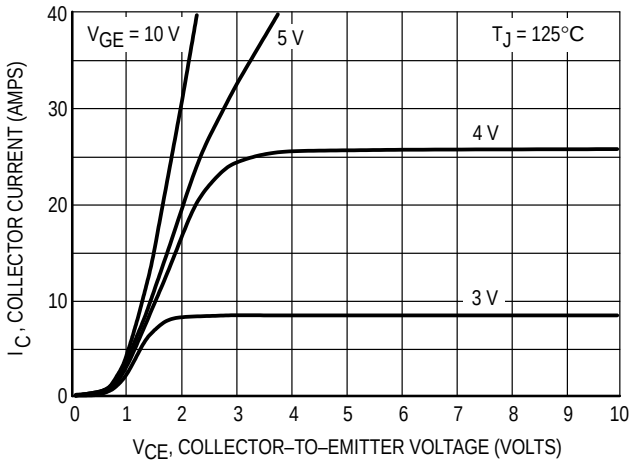


Figure 2. Output Characteristics, T_J = 125°C

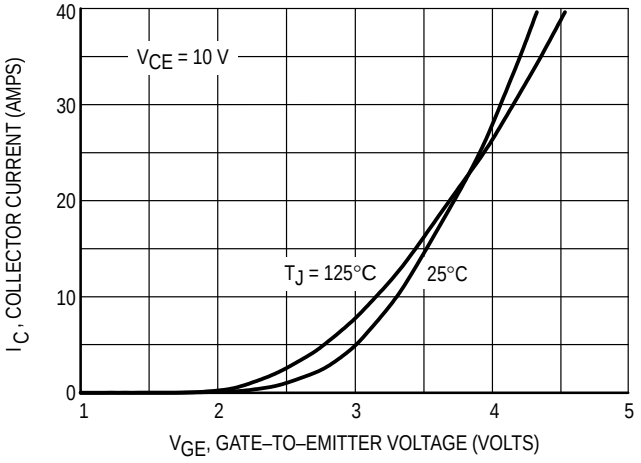


Figure 3. Transfer Characteristics

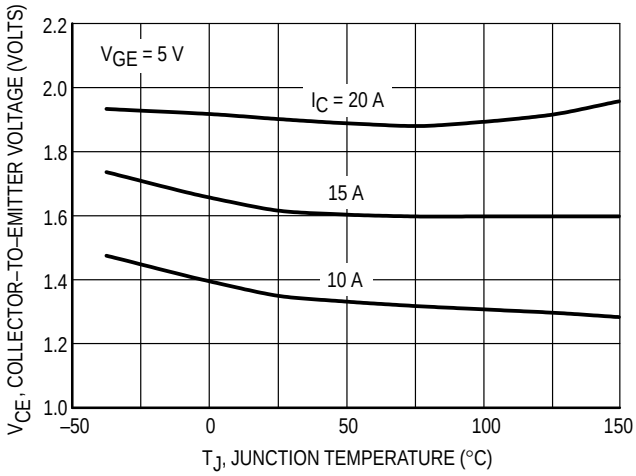


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

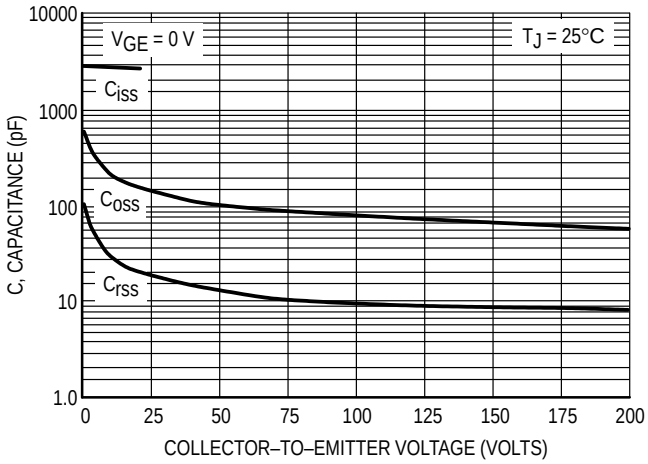


Figure 5. Capacitance Variation

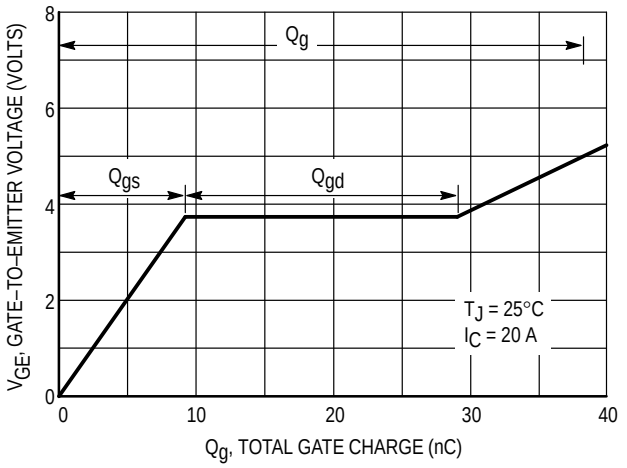


Figure 6. Gate–to–Emitter and Collector–to–Emitter Voltage vs Total Charge

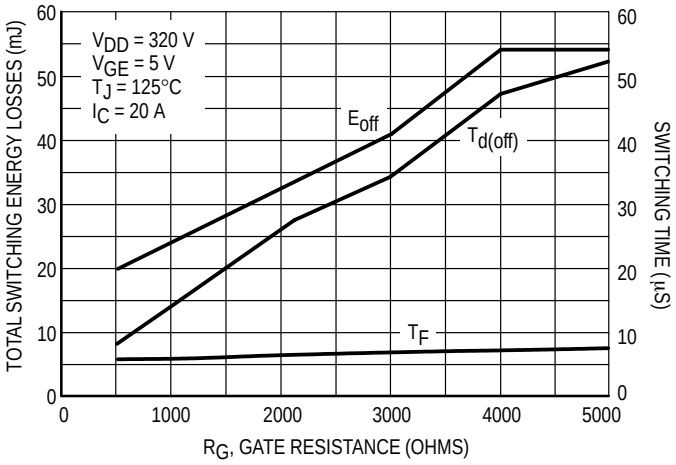


Figure 7. Total Switching Losses versus Gate Temperature

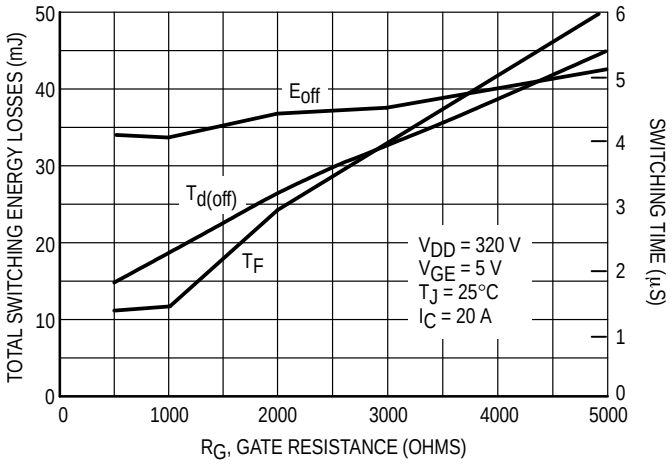


Figure 8. Total Switching Losses versus Gate Resistance

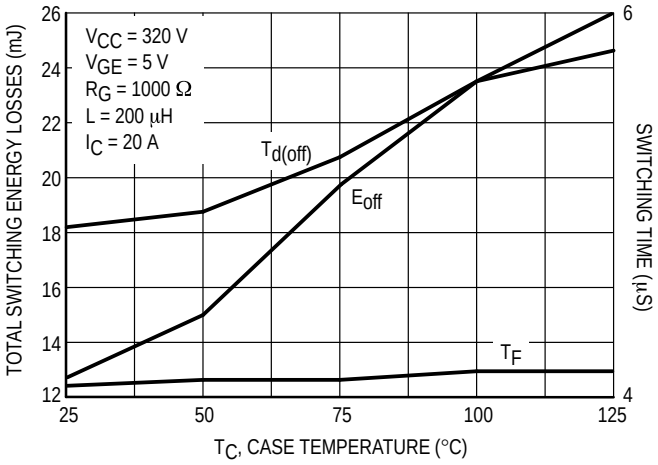


Figure 9. Total Switching Losses versus Case Temperature

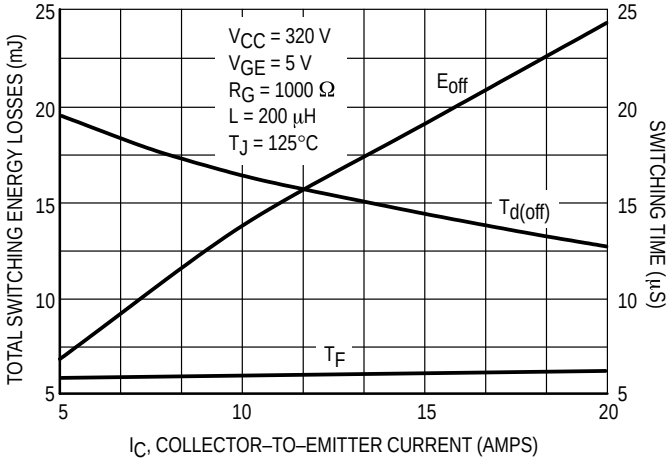


Figure 10. Total Switching Losses versus Collector Current

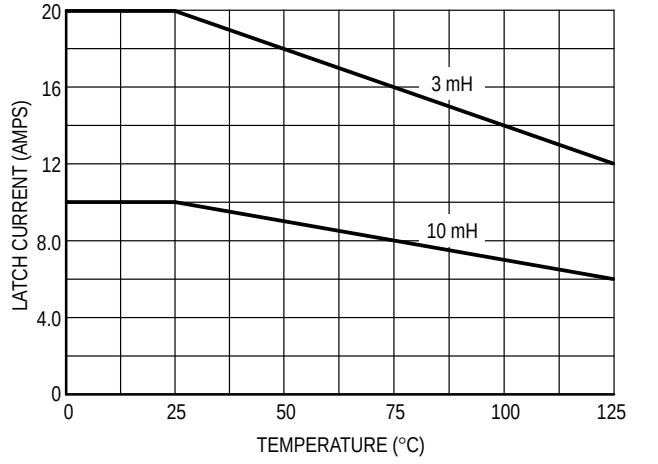


Figure 11. Latch Current versus Temperature

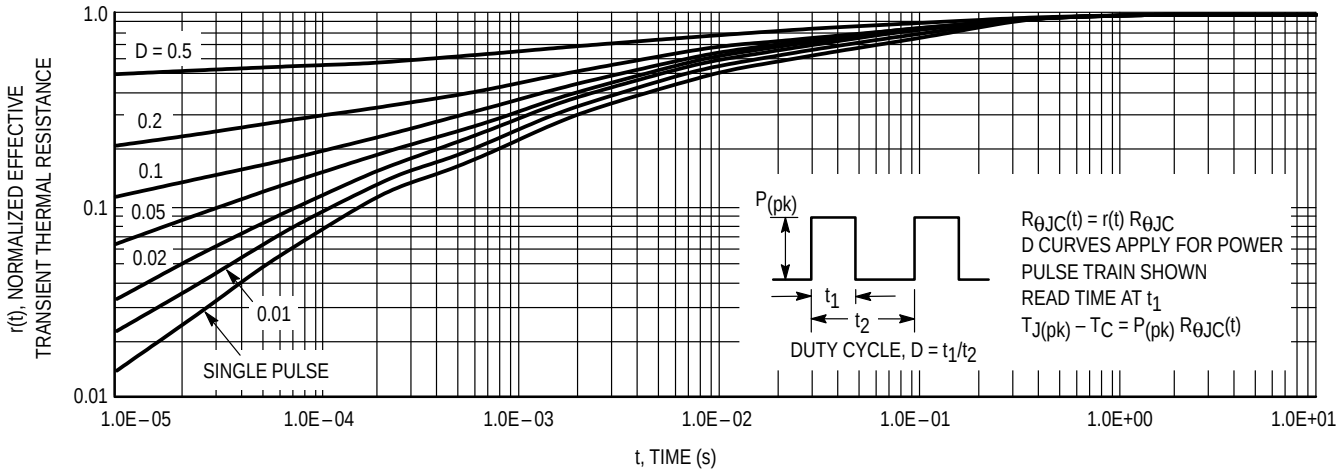
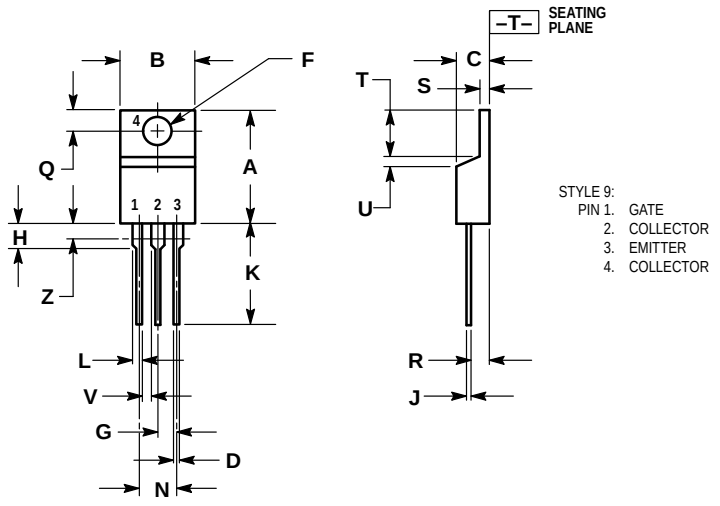


Figure 12. Thermal Response

PACKAGE DIMENSIONS



STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A–06
(TO–220AB)
ISSUE Y

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