International Rectifier

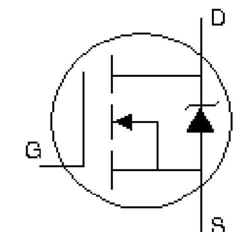
PD - 9.1336

PRELIMINARY

IRFR/U024N

HEXFET® Power MOSFET

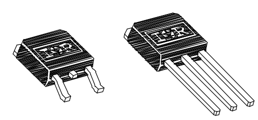
- Surface Mount (IRFR024N)
- Straight Lead (IRFU024N)
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

$R_{DS(on)}$ = 0.075Ω

I_D = 16A



D-PAK TO-252AA I-PAK TO-251AA

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	16	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	10	
I_{DM}	Pulsed Drain Current ①⑥	68	
P_D @T_C = 25°C	Power Dissipation	38	W
	Linear Derating Factor	0.30	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②⑥	71	mJ
I_{AR}	Avalanche Current①⑥	10	A
E_{AR}	Repetitive Avalanche Energy①	3.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	6.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

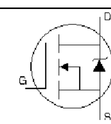
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	——	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	——	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.054	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.075	Ω	V_{GS} = 10V, I_D = 9.6A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	4.5	——	——	S	V_{DS} = 25V, I_D = 10A⑥
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	20	nC	I_D = 10A
Q_{gs}	Gate-to-Source Charge	——	——	5.3		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	7.6		V_{GS} = 10V, See Fig. 6 and 12 ④⑥
$t_{d(on)}$	Turn-On Delay Time	——	4.9	——	ns	V_{DD} = 28V
t_r	Rise Time	——	34	——		I_D = 10A
$t_{d(off)}$	Turn-Off Delay Time	——	19	——		R_G = 24Ω
t_f	Fall Time	——	27	——		R_D = 2.6Ω, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑤ 
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	370	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	140	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	65	——		*ƒ* = 1.0MHz, See Fig. 5⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	16	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	——	——	68		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 9.6A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	56	83	ns	T_J = 25°C, I_F = 10A
Q_{rr}	Reverse Recovery Charge	——	120	180	nC	di/dt = 100A/µs ④⑥

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 1.0mH R_G = 25Ω, I_{AS} = 10A. (See Figure 12)

③ $I_{SD} \le$ 10A, di/dt ≤ 280A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

⑥ Uses IRFZ24N data and test conditions.

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

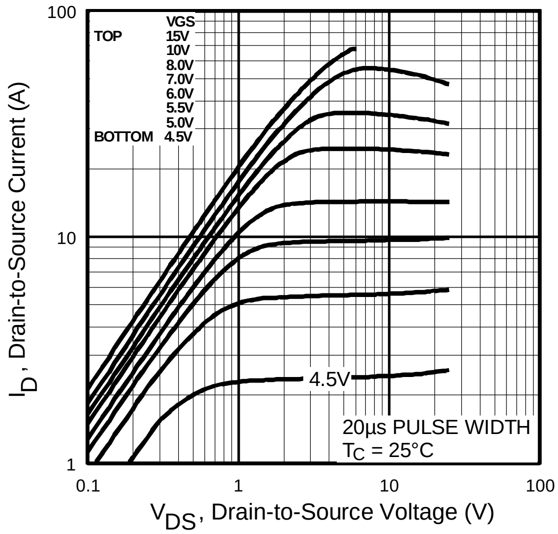


Fig 1. Typical Output Characteristics, $T_J = 25^oC$

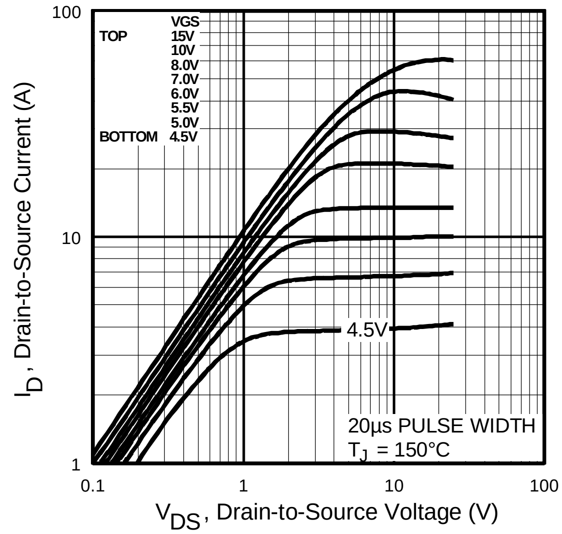


Fig 2. Typical Output Characteristics, $T_J = 150^oC$

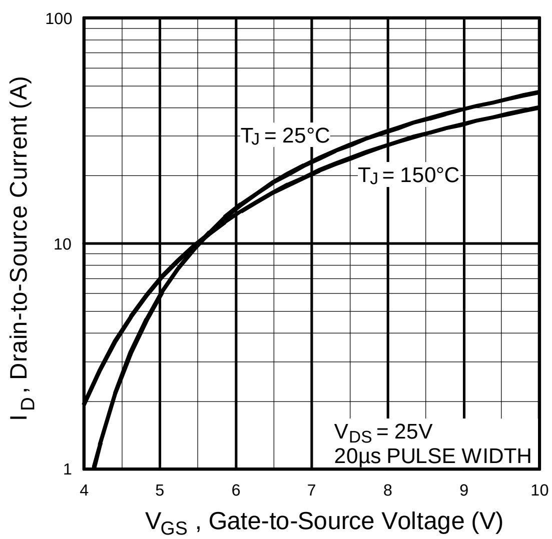


Fig 3. Typical Transfer Characteristics

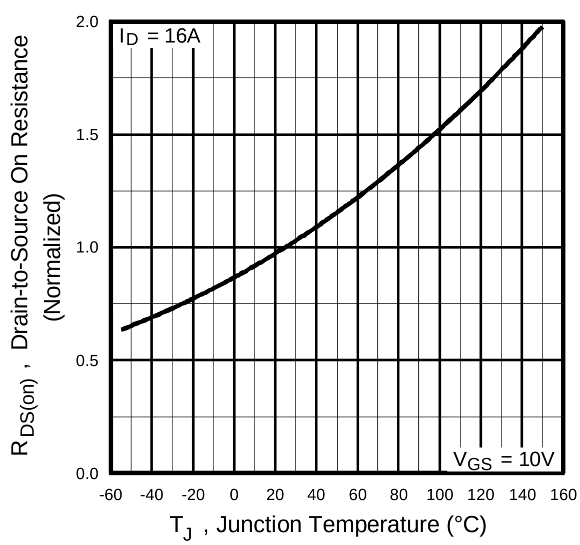


Fig 4. Normalized On-Resistance Vs. Temperature

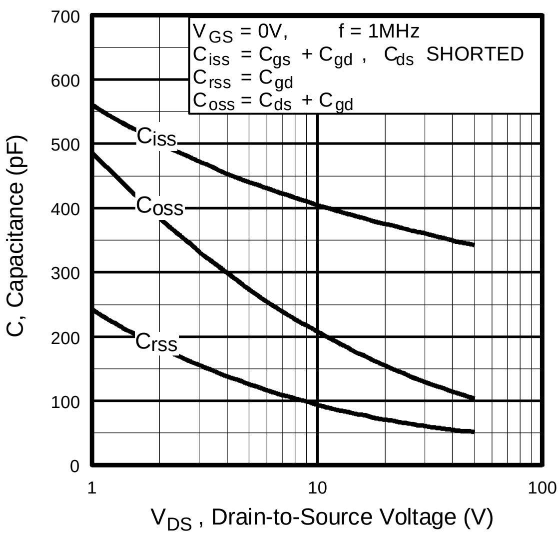


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

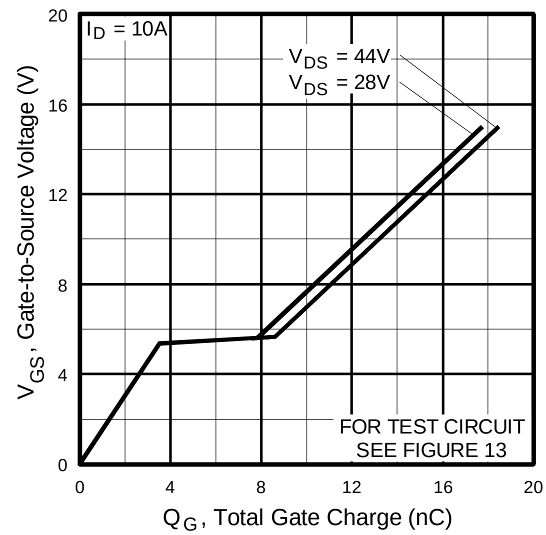


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

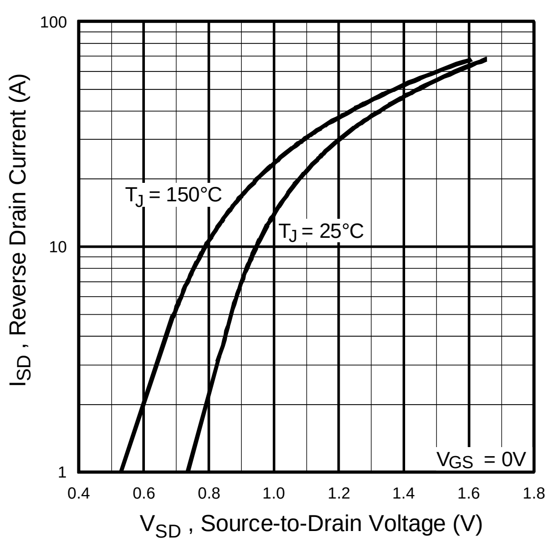


Fig 7. Typical Source-Drain Diode Forward Voltage

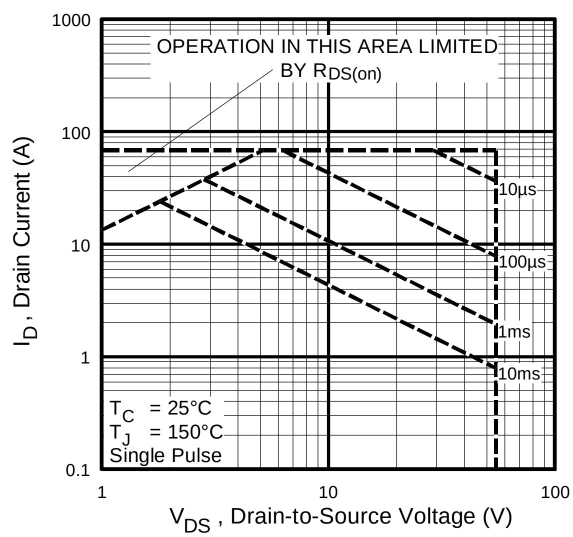


Fig 8. Maximum Safe Operating Area

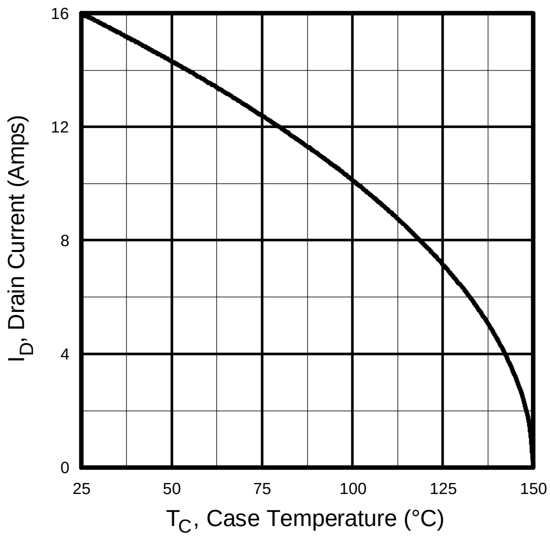


Fig 9. Maximum Drain Current Vs. Case Temperature

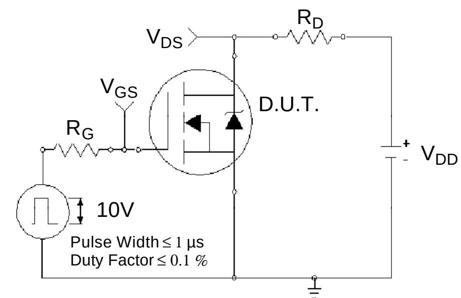


Fig 10a. Switching Time Test Circuit

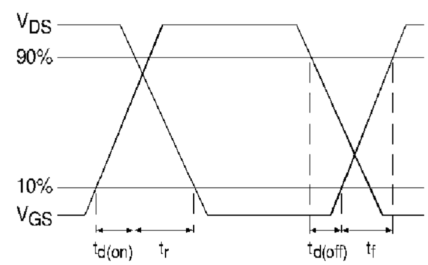


Fig 10b. Switching Time Waveforms

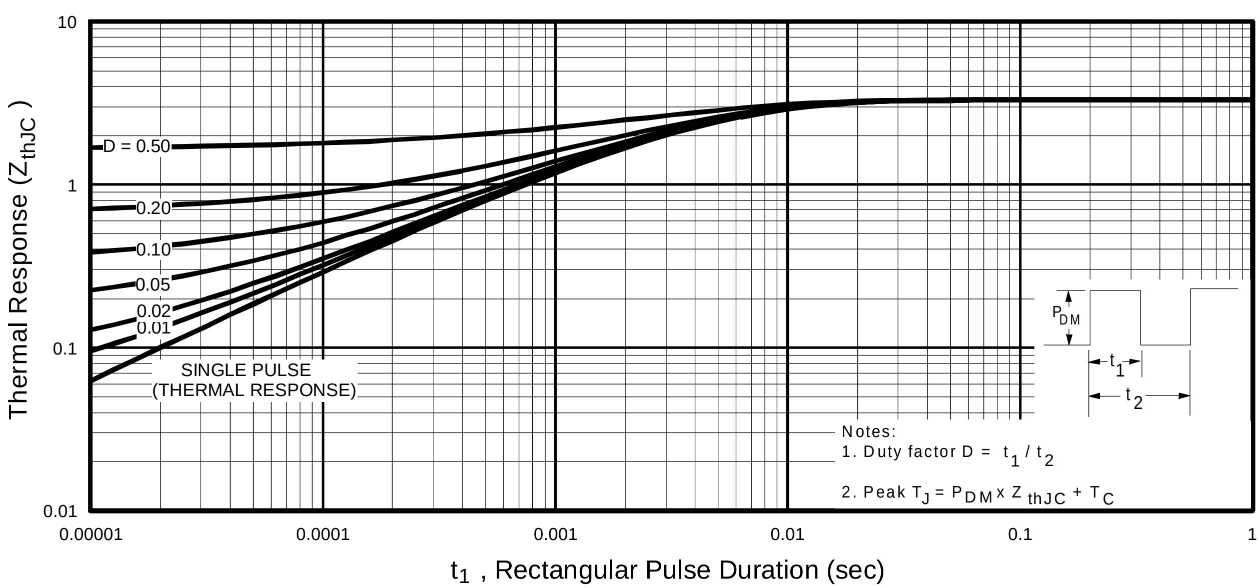


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

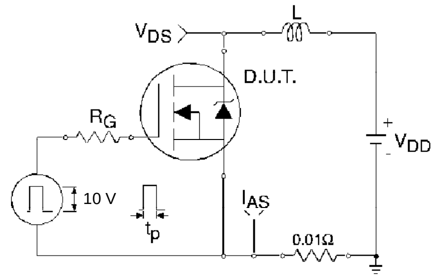


Fig 12a. Unclamped Inductive Test Circuit

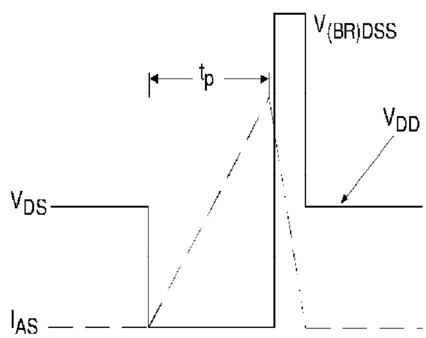


Fig 12b. Unclamped Inductive Waveforms

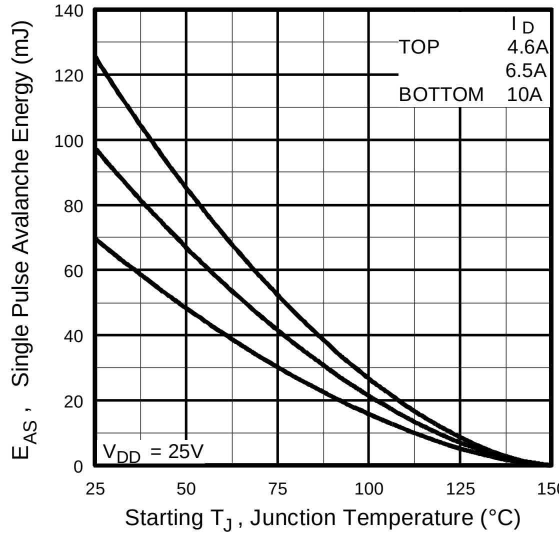


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

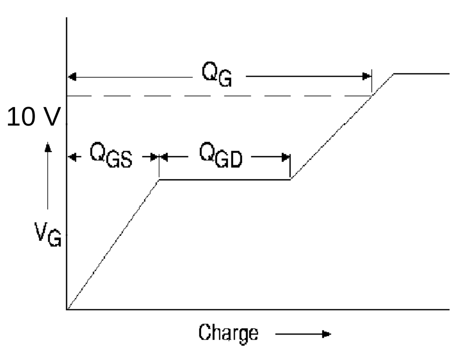


Fig 13a. Basic Gate Charge Waveform

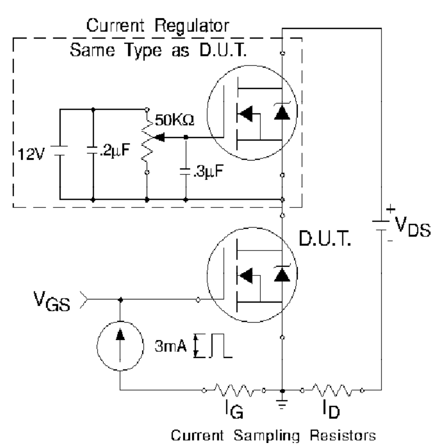
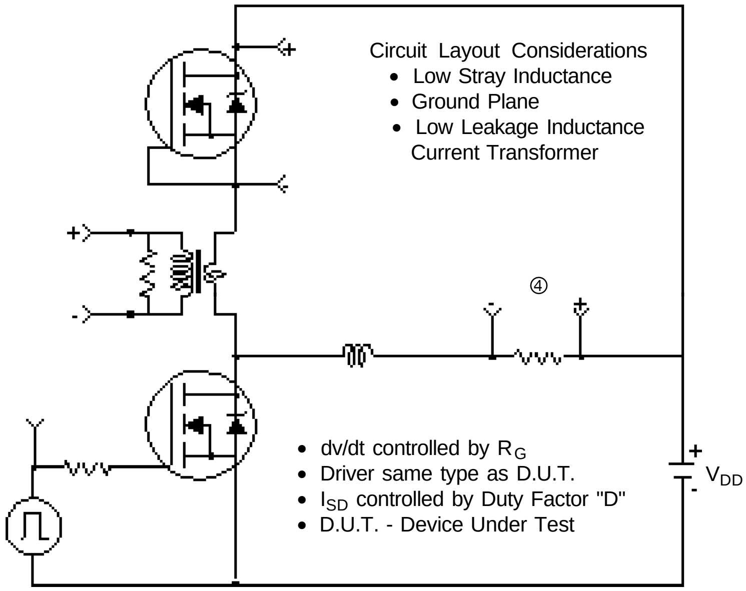
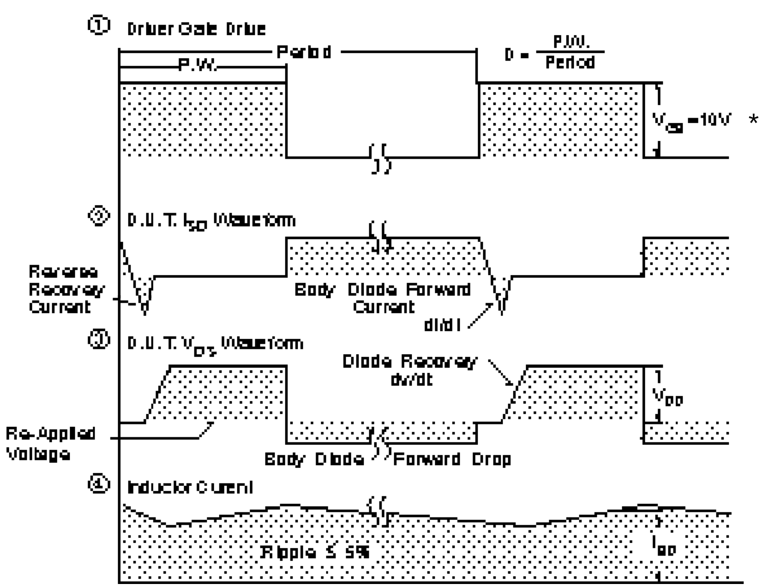


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit





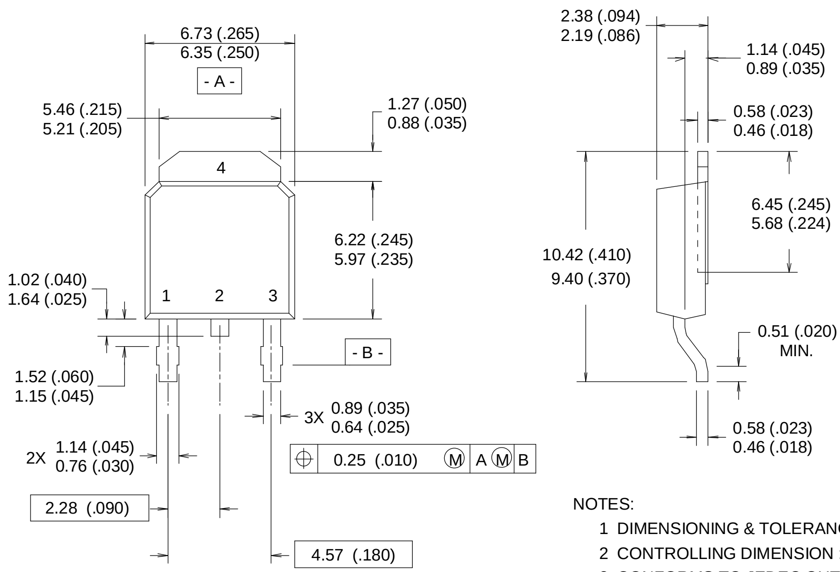
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-252AA Outline

Dimensions are shown in millimeters (inches)



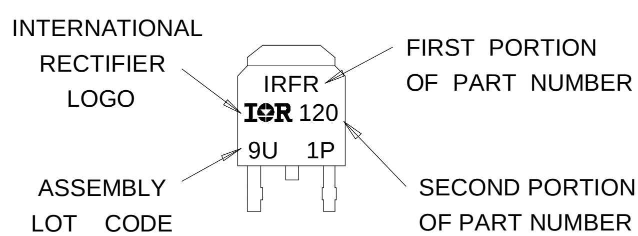
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

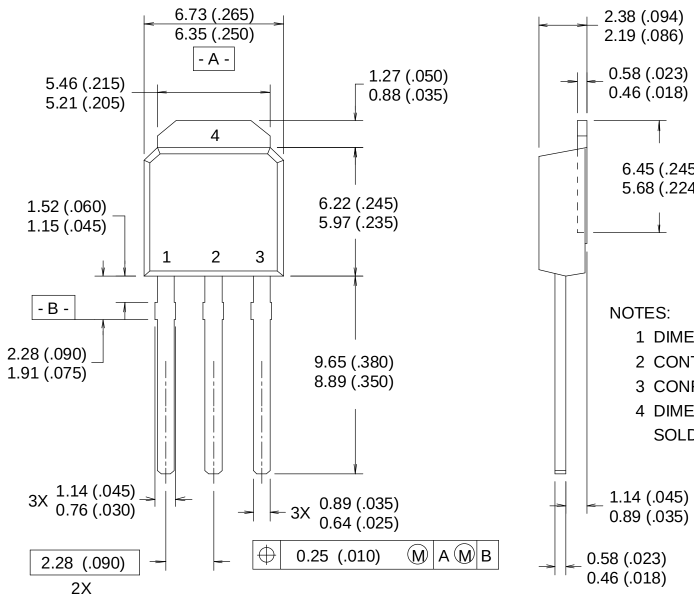
TO-252AA (D-PAK)

EXAMPLE : THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 9U1P



Package Outline

TO-251AA Outline
Dimensions are shown in millimeters (inches)



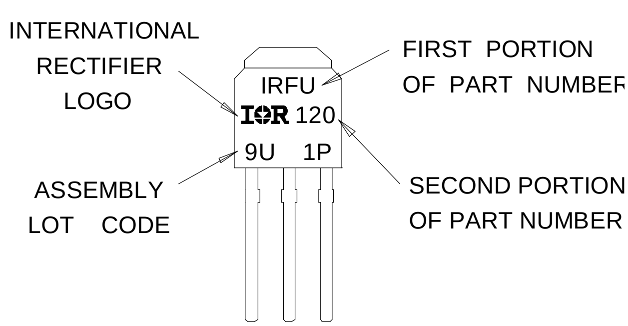
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

TO-251AA (I-PAK)

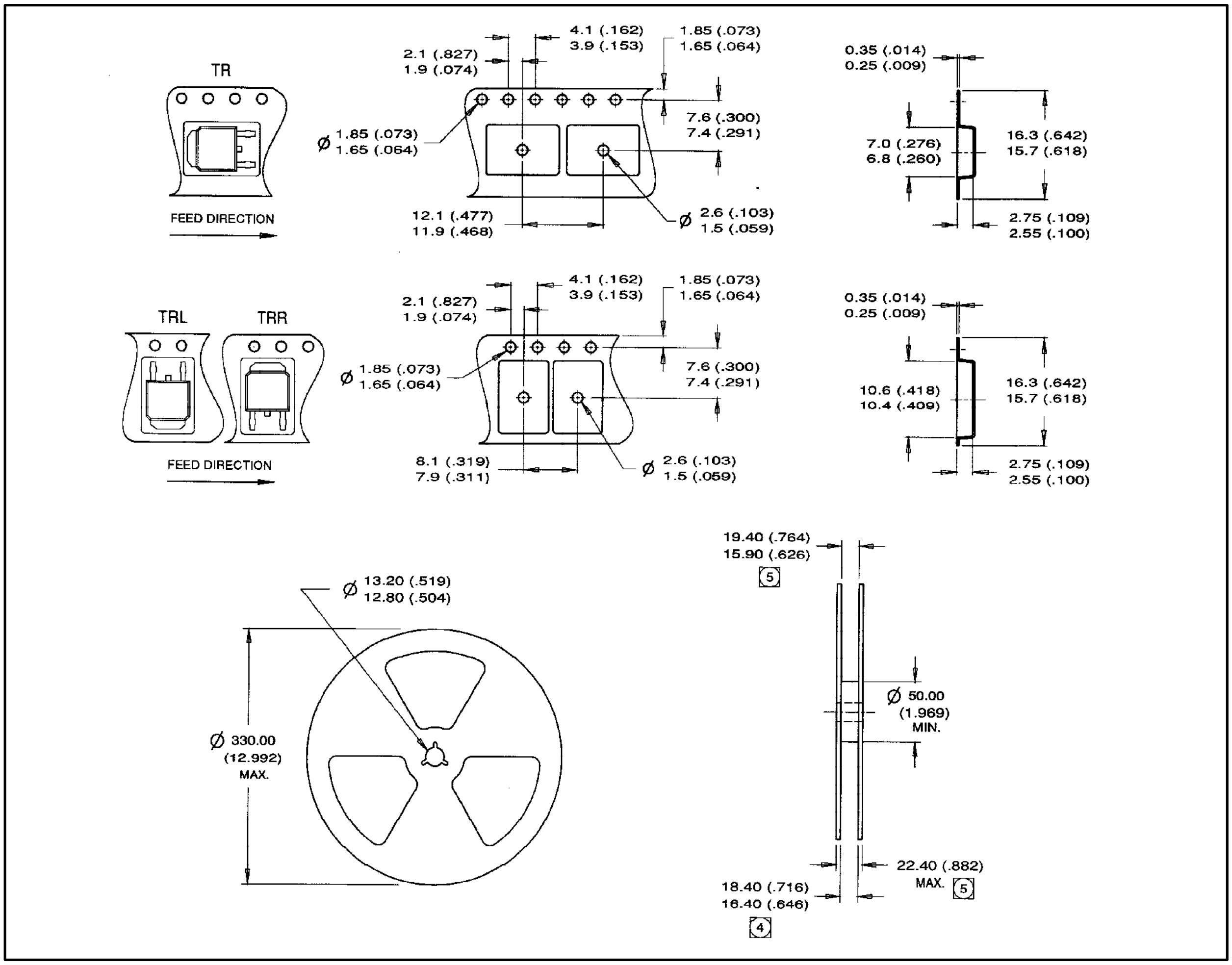
EXAMPLE : THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 9U1P



Tape & Reel Information

TO-252AA

Dimensions are shown in millimeters (inches)



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