CA3140, CA3140A

4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

November 1996

Features

- **MOSFET Input Stage**
  - **Very High Input Impedance (Z_{IN}) -1.5TΩ (Typ)**
  - **Very Low Input Current (I_I) -10pA (Typ) at ±15V**
  - **Wide Common Mode Input Voltage Range (V_{ICR}) - Can be Swung 0.5V Below Negative Supply Voltage Rail**
  - **Output Swing Complements Input Common Mode Range**
- **Directly Replaces Industry Type 741 in Most Applications**

Applications

- **Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation**
- **Sample and Hold Amplifiers**
- **Long Duration Timers/Multivibrators (μseconds-Minutes-Hours)**
- **Photocurrent Instrumentation**
- **Peak Detectors**
- **Active Filters**
- **Comparators**
- **Interface in 5V TTL Systems and Other Low Supply Voltage Systems**
- **All Standard Operational Amplifier Applications**
- **Function Generators**
- **Tone Controls**
- **Power Supplies**
- **Portable Instruments**
- **Intrusion Alarm Systems**

Description

The CA3140A and CA3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The CA3140A and CA3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

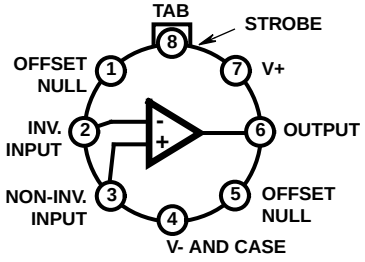
The CA3140 Series has the same 8-lead pinout used for the “741” and other industry standard op amps. The CA3140A and CA3140 are intended for operation at supply voltages up to 36V (±18V).

Ordering Information

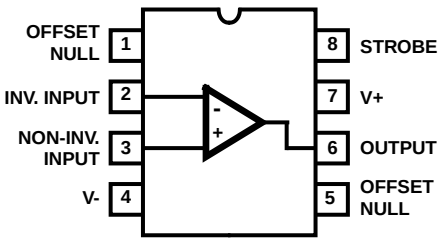
PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3140AE	-55 to 125	8 Ld PDIP	E8.3
CA3140AM (3140A)	-55 to 125	8 Ld SOIC	M8.15
CA3140AS	-55 to 125	8 Pin Metal Can	T8.C
CA3140AT	-55 to 125	8 Pin Metal Can	T8.C
CA3140E	-55 to 125	8 Ld PDIP	E8.3
CA3140M (3140)	-55 to 125	8 Ld SOIC	M8.15
CA3140M96 (3140)	-55 to 125	8 Ld SOIC Tape and Reel	
CA3140T	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA3140 (METAL CAN)
TOP VIEW



CA3140 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **957.3**

Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals) 36V
Differential Mode Input Voltage 8V
DC Input Voltage . . . . . (V+ +8V) To (V- -0.5V)
Input Terminal Current 1mA
Output Short Circuit Duration° (Note 2) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	100	N/A
SOIC Package	160	N/A
Metal Can Package	170	85

Maximum Junction Temperature (Metal Can Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Short circuit may be applied to ground or to either supply.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		TYPICAL VALUES CA3140	TYPICAL VALUES CA3140A	UNITS
Input Offset Voltage Adjustment Resistor		Typical Value of Resistor Between Terminals 4 and 5 or 4 and 1 to Adjust Max V_{IO}		4.7	18	kΩ
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage, (See Figure 27)	e_N	BW = 140kHz, R_S = 1MΩ		48	48	µV
Equivalent Input Noise Voltage (See Figure 35)	e_N	R_S = 100Ω	f = 1kHz	40	40	$nV/\sqrt{Hz}$
			f = 10kHz	12	12	$nV/\sqrt{Hz}$
Short Circuit Current to Opposite Supply	I_{OM}^+		Source	40	40	mA
	I_{OM}^-		Sink	18	18	mA
Gain-Bandwidth Product, (See Figures 6, 30)	f_T			4.5	4.5	MHz
Slew Rate, (See Figure 31)	SR			9	9	V/µs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	µA
Transient Response (See Figure 28)	t_r	R_L = 2kΩ, C_L = 100pF	Rise Time	0.08	0.08	µs
	OS		Overshoot	10	10	%
Settling Time at $10V_{P-P}$, (See Figure 5)	t_S	R_L = 2kΩ, C_L = 100pF, Voltage Follower	To 1mV	4.5	4.5	µs
			To 10mV	1.4	1.4	µs

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	CA3140 MIN	CA3140 TYP	CA3140 MAX	CA3140A MIN	CA3140A TYP	CA3140A MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$	-	5	15	-	2	5	mV
Input Offset Current	$\|I_{IO}\|$	-	0.5	30	-	0.5	20	pA
Input Current	I_I	-	10	50	-	10	40	pA
Large Signal Voltage Gain (Note 3) (See Figures 6, 29)	A_{OL}	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB
Common Mode Rejection Ratio (See Figure 34)	CMRR	-	32	320	-	32	320	µV/V
		70	90	-	70	90	-	dB
Common Mode Input Voltage Range (See Figure 8)	V_{ICR}	-15	-15.5 to +12.5	11	-15	-15.5 to +12.5	12	V

Electrical Specifications For Equipment Design, at V_{SUPPLY} = ±15V, T_A = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	CA3140			CA3140A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 36)	PSRR	-	100	150	-	100	150	µV/V
		76	80	-	76	80	-	dB
Max Output Voltage (Note 4) (See Figures 2, 8)	V_{OM}+	+12	13	-	+12	13	-	V
	V_{OM}-	-14	-14.4	-	-14	-14.4	-	V
Supply Current (See Figure 32)	I+	-	4	6	-	4	6	mA
Device Dissipation	P_D	-	120	180	-	120	180	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	8	-	-	6	-	µV/°C

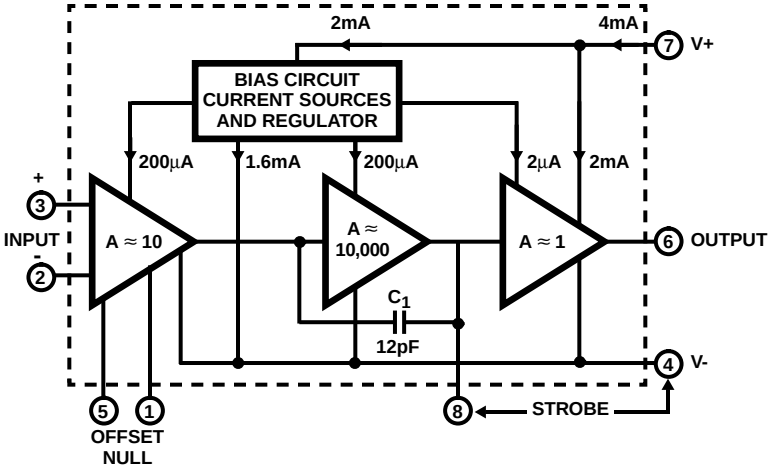
NOTES:

3. At V_O = 26V_{P-P}, +12V, -14V and R_L = 2kΩ.
4. At R_L = 2kΩ.

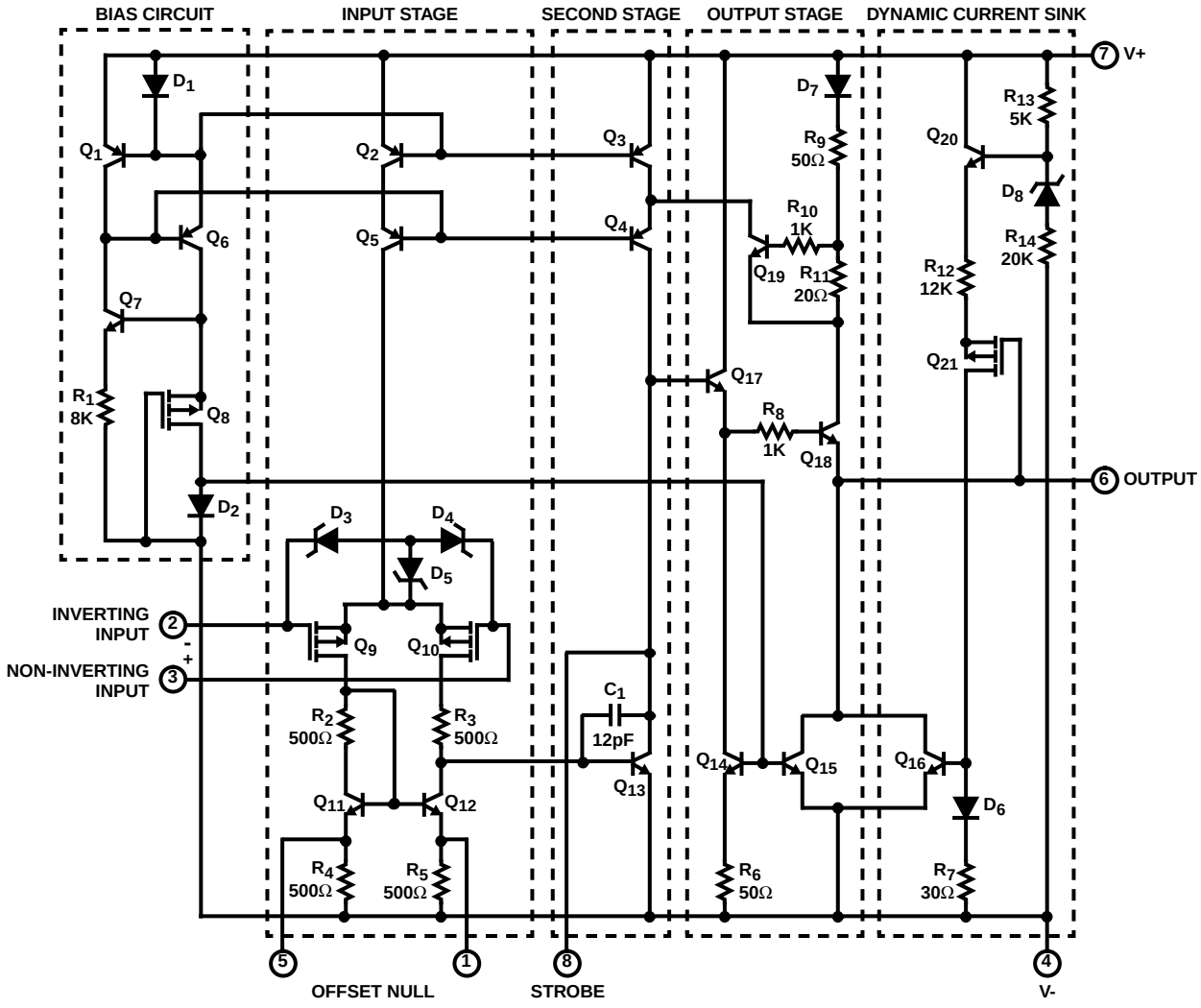
Electrical Specifications For Design Guidance At V+ = 5V, V- = 0V, T_A = 25°C

PARAMETER		SYMBOL	TYPICAL VALUES		UNITS
			CA3140	CA3140A	
Input Offset Voltage		$\|V_{IO}\|$	5	2	mV
Input Offset Current		$\|I_{IO}\|$	0.1	0.1	pA
Input Current		I_I	2	2	pA
Input Resistance		R_I	1	1	TΩ
Large Signal Voltage Gain (See Figures 6, 29)		A_{OL}	100	100	kV/V
			100	100	dB
Common Mode Rejection Ratio		CMRR	32	32	µV/V
			90	90	dB
Common Mode Input Voltage Range (See Figure 8)		V_{ICR}	-0.5	-0.5	V
			2.6	2.6	V
Power Supply Rejection Ratio		PSRR $\Delta V_{I0}/\Delta V_S$	100	100	µV/V
			80	80	dB
Maximum Output Voltage (See Figures 2, 8)		V_{OM}+	3	3	V
		V_{OM}-	0.13	0.13	V
Maximum Output Current:	Source	I_{OM}+	10	10	mA
	Sink	I_{OM}-	1	1	mA
Slew Rate (See Figure 31)		SR	7	7	V/µs
Gain-Bandwidth Product (See Figure 30)		f_T	3.7	3.7	MHz
Supply Current (See Figure 32)		I+	1.6	1.6	mA
Device Dissipation		P_D	8	8	mW
Sink Current from Terminal 8 to Terminal 4 to Swing Output Low			200	200	µA

Block Diagram



Schematic Diagram



NOTE: All resistance values are in ohms.

Typical Performance Curves

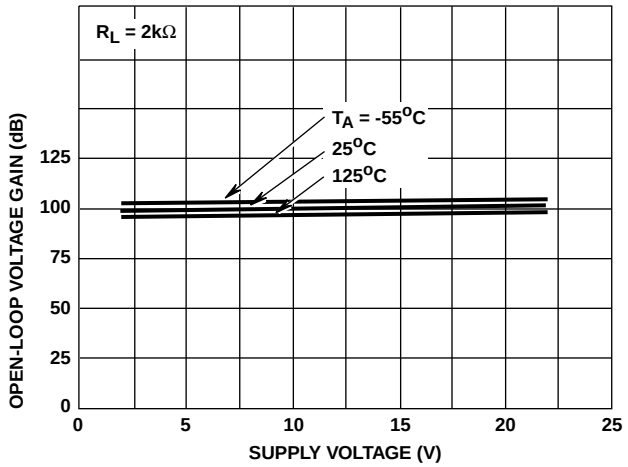


FIGURE 29. OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE AND TEMPERATURE

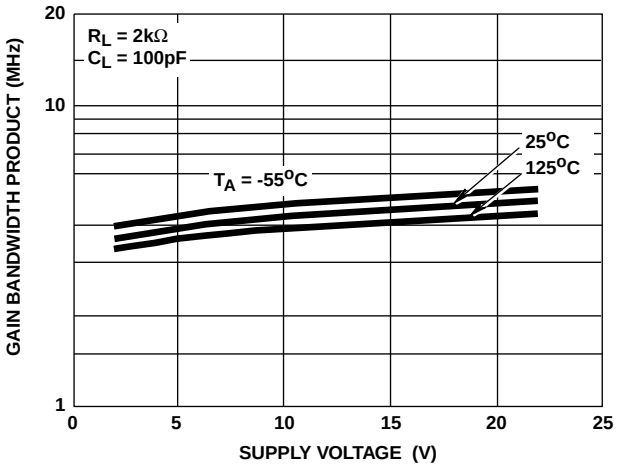


FIGURE 30. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE AND TEMPERATURE

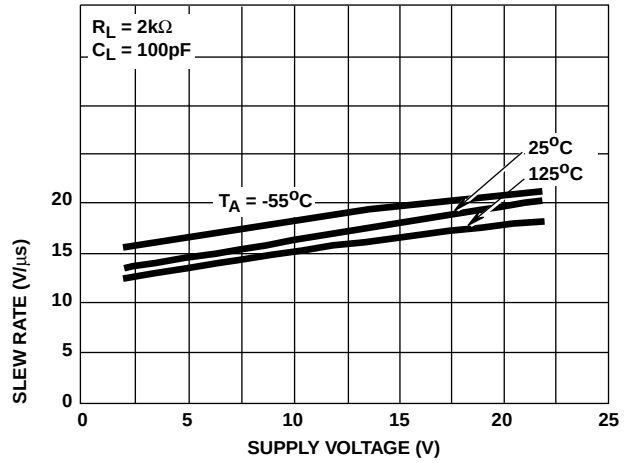


FIGURE 31. SLEW RATE vs SUPPLY VOLTAGE AND TEMPERATURE

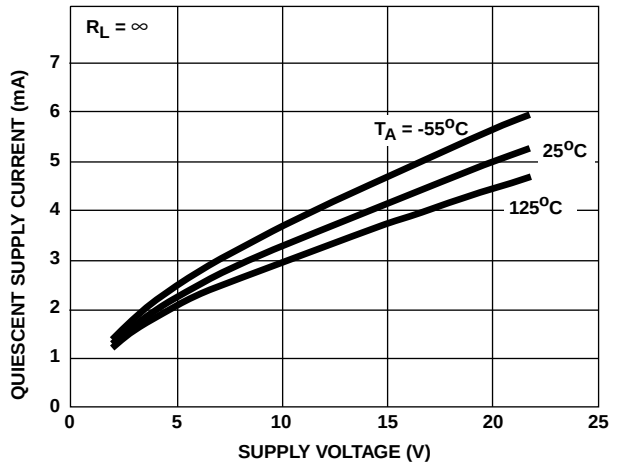


FIGURE 32. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

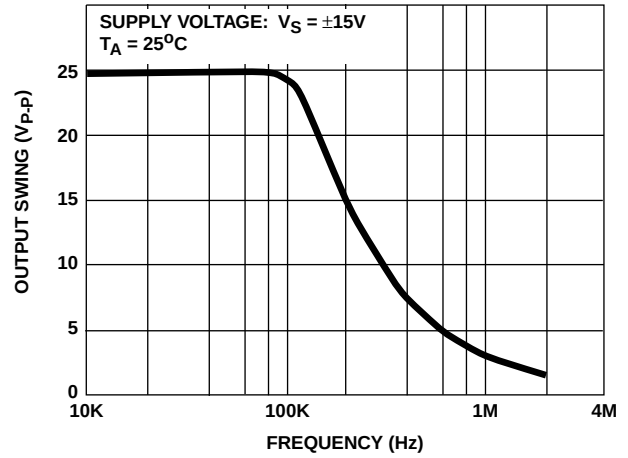


FIGURE 33. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

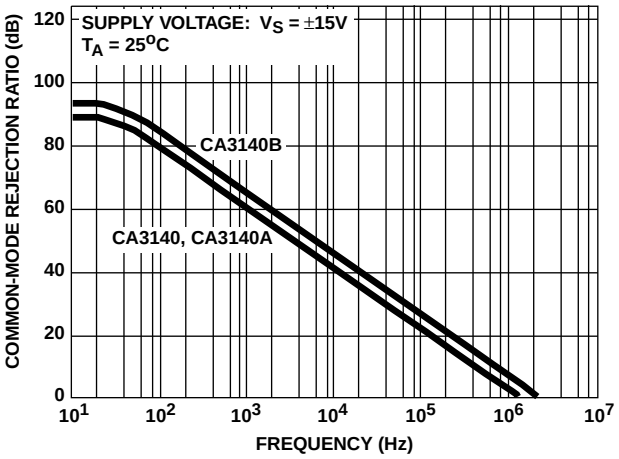


FIGURE 34. COMMON MODE REJECTION RATIO vs FREQUENCY

Typical Performance Curves (Continued)

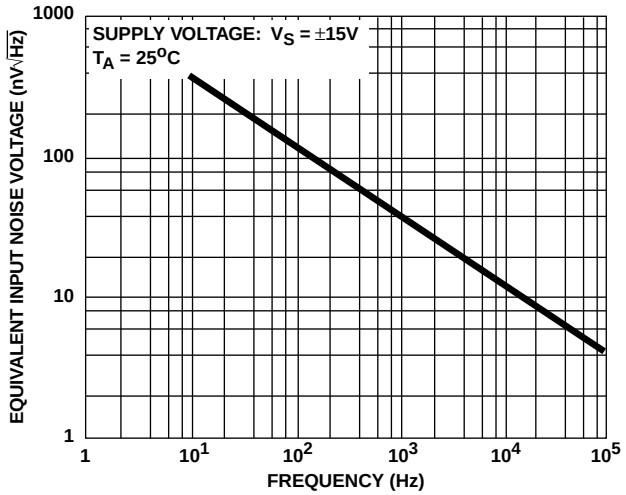


FIGURE 35. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

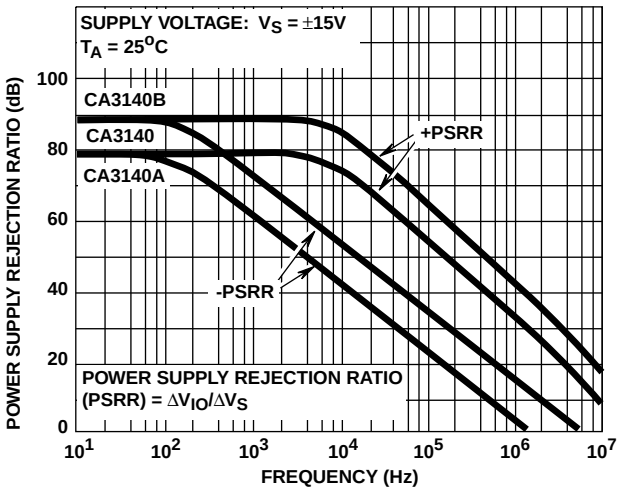
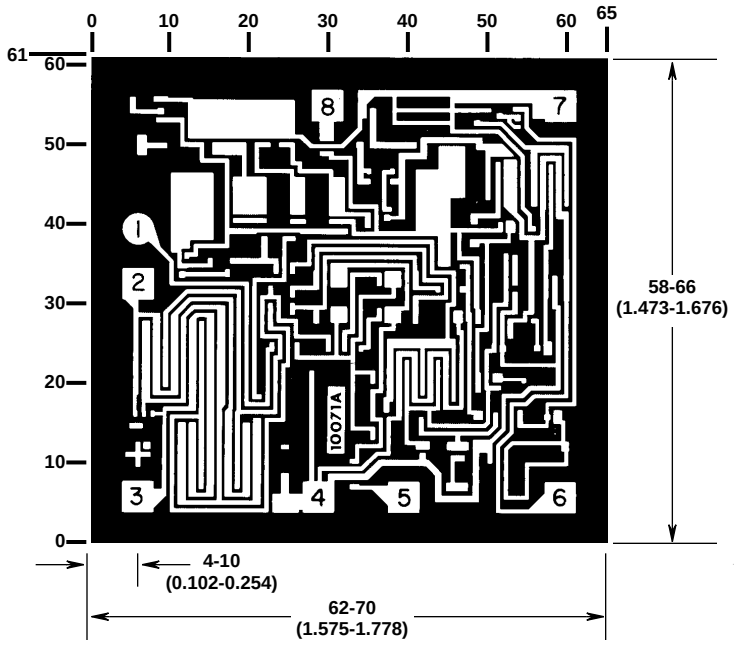


FIGURE 36. POWER SUPPLY REJECTION RATIO vs FREQUENCY

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.